Single-Phase PLL Based on an Adaptive Notch Filter

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Abstract. *Single-Phase Phase-Locked Loops (PLL) have become a crucial component of grid-tied power converters. PLL accuracy and fast response are important for control and protection purposes, especially in the presence of voltage harmonics and frequency variations. In this paper, a new PLL structure based on an Adaptive Notch Filter (ANF) is presented. This ANF, which generates the orthogonal system of the PLL, is implemented with an All-Pass Filter (APF) having inherent advantages, such as low sensitivity to coefficient rounding when implemented in fixed-point microprocessors and easy implementation in a Digital Signal Processing (DSP). Both simulation with MATLAB/Simulink, and experimental results on a fixed-point DSP, are presented and analyzed to evaluate the performance of the introduced PLL and to support the theoretical development. A set of comparative simulations between the proposed PLL and a some single-phase PLL described in the literature are conducted to validate the method.*

Keywords

Adaptive Notch Filter, All-Pass Filter, Orthogonal Signal Generator, Phase-Locked Loop, Single-Phase PLL.

1. Introduction

Distributed Energy Resources (DERs) have become increasingly widespread in recent years. This has increased grid connection requirements of renewable energy sources e.g. wind or solar. The control of power electronics front ends has been improved in order to meet new standards and grid codes [1] and [2]. In order to meet the new requirements, researches have focused on synchronization and control techniques of renewable energy powered grid-connected converters [3]. The grid synchronization is based on the detection of the voltage phase angle at the Point of Common Coupling (PCC). Synchronization must be accurate and fast, even in the presence of grid disturbances such as line harmonics, voltage sags/swell/loss, frequency variations and phase jumps [4].

Among DERs, single-phase ones have only recently gained interest [5], and the PLL topology has emerged as de facto phase detection structure. Information regarding the condition of the grid is scarcer in single-phase systems than in three-phase systems [6]. Hence, more advanced methods should be considered to create an orthogonal voltage system which makes it possible to obtain the voltage phase angle at the PCC. Apart from single-phase DERs, such as photovoltaic inverters [7] and energy storage devices, all single-phase power electronic front ends, like Uninterruptible Power Supplies (UPS) or regenerative drives, need a PLL in their control loop [8] and [9]. With the voltage phase angle at the PCC, the active and reactive current references of the inner current loop are calculated so that the power factor of the device has the design value. Moreover, the PLL should provide instantaneous Root Mean Square (RMS) voltage, and it would be very interesting if it could provide grid frequency, too. Both magnitudes are usually needed for both active and passive anti-islanding detection algorithms in photovoltaic inverters [10] or in the droop method for converter parallel operation [11].

General structure of a single-phase PLL for grid synchronization is presented in [12]. The most important component is the orthogonal system generator, and the

main difference among all PLLs proposed in the literature lies precisely in this element. The orthogonal system can be generated in several ways [13]. The methods commonly found in the technical literature use the transport delay block [14], Hilbert transformation, Moving Average Filter (MAF) with variable sampling time, such as in [15] or constant sample time [16], and inverse Park transformation as in [17] and [18]. However, these techniques have one or more of the following shortcomings: frequency dependence, high complexity, non-linearity, and poor or no noise filtering capability.

A single-phase PLL structure based on a Second Order Generalized Integrator (SOGI) which overcomes all the aforementioned drawbacks was presented in [19] and [20], together with a filtering delay due to its resonance at the fundamental frequency. Rodriguez et al. [21] and [22] presented a three-phase PLL based on a Dual Second Order Generalized Integrator (DSOGI). The SOGI structure has also been applied to other aspects of power electronic control [23], mainly to the current control loop [24] and [25], harmonic detection [26] and even in active anti-islanding methods [27]. However, as already stated in [20] and later in [24], since the SOGI structure was designed in the continuous time, its discrete implementation has amplitude ripples and phase delays different from the quadrature. Moreover, it requires a lot of resources to implement in a fixed-point DSP or Field-Programmable Gate Array (FPGA) due to its limited accuracy and sensitivity to coefficient rounding.

Continuous time notch filters and their adaptive version ANF, have long been used as frequency detectors [28], especially in single-phase systems [29]. Only recently have they started being used as orthogonal system generators, especially in the continuous time domain [30]. Besides having the same drawbacks as the SOGI structure, ANF does not provide any unity gain orthogonal system generator but one whose gain depends on the 3 dB band pass of the filter. This drawback, which is common to both the continuous and discrete time versions of ANF, does not allow the use of traditional ANF as PLL despite being a good candidate.

In this paper, a new single-phase PLL based on a second order Normalized Digital APF is presented. An APF is like a versatile DSP building block with the best characteristics for notch filter [31] and adaptive notch filter applications. In order to provide a unity gain orthogonal system, the authors propose a normalization method which provides two orthogonal signals (the in-phase and the quadrature one) with the same amplitude of the input, just as traditional PLL implementations do, but without the above drawbacks.

This paper is organized as follows. In Sec. 2. , an overview of the whole system is given. Section 3. describes the APF and its application to the ANF. The normalization of the ANF is described in Sec. 4. while in Sec. 5. some implementation issues are presented. Next, simulation and experimental results are provided in Sec. 4. Section 7. presents a comparison study with others PLLs. Finally, Sec. 8. draws conclusions.

2. Overview of Single-Phase PLL

According to Fig. 1, Single-Phase PLLs are mainly composed of two blocks: a first block which generates an orthogonal system (with one of its components in phase and a second component lagging $\pi/2$ the input single-phase voltage) and a second block which computes the angle and voltage magnitude from the orthogonal system [32]. The most important role is played by the orthogonal system generator, where the main differences lie between all PLLs in the literature. The rest of the blocks are the same as in most PLL implementations.

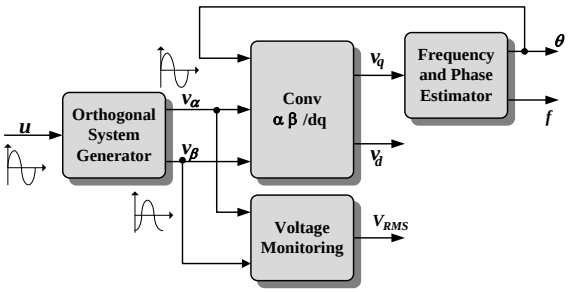


Fig. 1: Structure of a single PLL.

A second order ANF based on a discrete APF seems a good candidate as the orthogonal system generator due to its low sensitivity to coefficient rounding and loss-less internal structure, very suitable for adaptive algorithms [33]. Furthermore, the computational cost of implementation is quite low, especially in the state-space representation.

In order to allow extraction of the voltage amplitude by the second block, the transfer function from the magnitude of the input voltage to both output orthogonal signals of the ANF must have either a unity magnitude or a known constant gain. This is not true of traditional ANF, although they have a gain different from unity which depends, among other factors, on the 3 dB band pass of the filter. This important drawback of traditional ANF is the main reason why they have not been used in single PLL so far. The next sections describe a normalization of the ANF which meets the above requirements while generating a unity gain orthogonal system (that is, it generates an orthonormal system).

3. APF: DSP Building Block

Digital APF was analyzed in detail in [31], and hence they are briefly described for the sake of completeness. The frequency response of an APF has unity magnitude at all frequencies:

$$\left|A(e^{j\omega})\right|^2 = 1, \text{ for all } \omega. \tag{1}$$

Transfer functions of APF have all poles and zeroes as conjugate reciprocal pairs. If the transfer function is constrained to be a real function, then the numerator polynomial is obtained from the denominator by reversing the order of the coefficients. Among all implementation structures for discrete filters, the normalized lattice structure (Fig. 2) is the most useful for real coefficient, second order filters as all internal nodes are automatically scaled (coefficients are less than or equal to 1), which is a suitable characteristic for fixed-point DSP implementation [31] and [34]. In Fig. 2, $u(n)$ is the input signal and $y_f(n)$ is the output filtered signal, $A(n)$ is the filter transfer functions and $x_1(n)$ and $x_2(n)$ are the two orthogonal components.

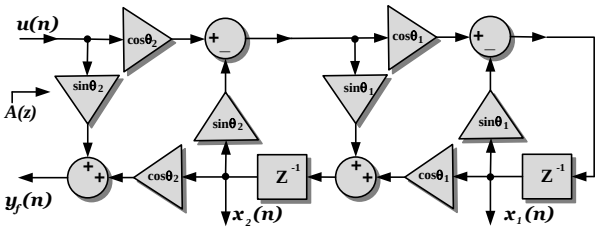


Fig. 2: Second order All-Pass Filter implemented in a normalized lattice structure.

A second order APF transfer function can then be expressed as:

$$A(z) = \frac{k_2 + k_1(1+k_2)z^{-1} + z^{-2}}{1 + k_1(1+k_2)z^{-1} + k_2 z^{-2}}. \tag{2}$$

Considering that all internal nodes are less than or equal to 1, we can make the following changes to Eq. (2), $k_1 = \sin\theta_1$ and $k_2 = \sin\theta_2$, where θ_1 and θ_2 can be further expressed as:

$$\theta_1 = \frac{\omega_0}{f_s} - \frac{\pi}{2}, \tag{3}$$

$$\theta_2 = \arcsin\left(\frac{1 - \tan\left(\frac{BW}{2}\right)}{1 + \tan\left(\frac{BW}{2}\right)}\right), \tag{4}$$

where ω_0 is the so called notch frequency, and $BW = 2\pi B \cdot f_s^{-1}$, is the so called band width of the filter, with B being the band pass and f_s the sampling frequency. Finally, we obtain:

$$A(z) = \frac{\sin\theta_2 + \sin\theta_1(1+\sin\theta_2)z^{-1} + z^{-2}}{1 + \sin\theta_1(1+\sin\theta_2)z^{-1} + \sin\theta_2 z^{-2}}. \tag{5}$$

The lattice notch filter, expressed as Eq. (5), provides a decoupling between the notch frequency ω_0 and the 3 dB band pass of the filter. Decoupling is very useful in adaptive filters where it is necessary to adapt the notch or band pass frequency. This characteristic will be used later for obtaining an ANF [35]. Apart from having unity magnitude at all frequencies, the real coefficient, second order APF has zero phase shift for $\omega < \omega_0$ and π shift for $\omega = \omega_0$ whereas the rest have a phase shift of 2π.

As mentioned before, the APF is a versatile DSP building block. Furthermore, due to the π shift for $\omega = \omega_0$, it is easy to construct a Digital Notch Filter (DNF) and its complementary one (a band-pass filter) from the APF presented before (Fig. 3).

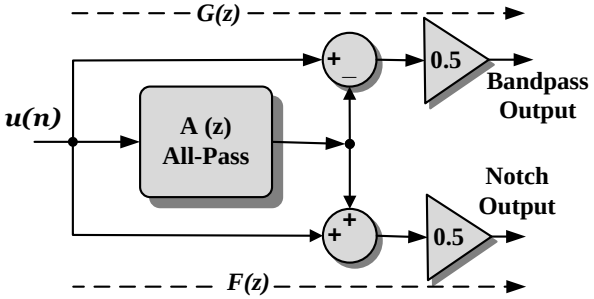


Fig. 3: Generation of a band-pass (G(z)) and notch (F(z)) filter based on an All-pass filter.

Notch and band-pass filter transfer functions can be obtained as:

$$F(z) = \frac{1}{2}[1 + A(z)], \tag{6}$$

$$G(z) = \frac{1}{2}[1 - A(z)]. \tag{7}$$

For our interest, only the transfer function of F(z) is given:

$$F(z) = \\ = \frac{1+\sin\theta_2+2\sin\theta_1(1+\sin\theta_2)z^{-1}+(1+\sin\theta_2)z^{-2}}{1+\sin\theta_1(1+\sin\theta_2)z^{-1}+\sin\theta_2 z^{-2}}. \tag{8}$$

The Notch Filter based on the APF of Eq. (6) and Eq. (7), has the particularity of generating an orthogonal system. Figure 2, where the lattice implementation of the APF is depicted, shows the two internal nodes x_1 and x_2. The transfer functions for both nodes are as follows:

$$x_1(n) = X_1(z)u(n), \tag{9}$$

$$X_1(z) = \frac{\cos\theta_1\cos\theta_2 z^{-1}}{1+\sin\theta_1(1+\sin\theta_2)z^{-1}+\sin\theta_2 z^{-2}}, \tag{10}$$

$$x_2(n) = X_2(z)u(n), \tag{11}$$

$$X_2(z) = \frac{\sin\theta_1\cos\theta_2 z^{-1} + \cos\theta_2 z^{-2}}{1+\sin\theta_1(1+\sin\theta_2)z^{-1}+\sin\theta_2 z^{-2}}. \tag{12}$$

Although these two internal nodes represent an orthogonal system (x_1 is lagging 0.5 π the input sinusoidal voltage and x_2 is in phase with the input sinusoidal voltage), their amplitudes are not directly related to the magnitude of the input voltage because the gain of their transfer functions at the notch frequency is different from unity.

For x_1 and x_2 to be an appropriate orthogonal system generator for a single PLL, the transfer functions must be previously normalized; that is, they must have a unity gain at the notch frequency. The following section presents a normalized version of Eq. (10) and Eq. (12).

Since the main purpose of a PLL is to extract the input voltage angle, it is also highly desirable to obtain other characteristics of the input voltage such as the instantaneous RMS voltage and frequency. In most cases, it is not only desirable but also necessary, as in solar Photovoltaic (PV) inverters implementing the anti-islanding algorithm [27], where a quick and precise estimate of the magnitude and main frequency is needed. Although the DNF in the previous section could extract the input voltage angle, if either the magnitude or the frequency of the input voltage must be extracted too, then an adaptation algorithm must be implemented. Figure 4, shows the structure of the proposed APF-PLL, with the three main blocks:

- the orthonormal generator based on an APF,
- the adaptation algorithm,
- last block, which extracts the input voltage angle and magnitude.

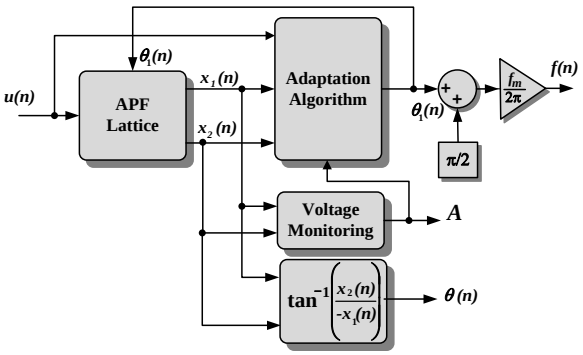


Fig. 4: Structure of the proposed APF-PLL.

This adaptation algorithm must make ω_0 (or by Eq. (3), its associated variable θ_1) converge towards the mains pulsation ω_e. In [33] and [36], Regalia proposed a stable and efficient lattice algorithm for adaptive Infinite Impulse Response (IIR) filtering but the adaptation performance depended on the amplitude of the signal. In [37], a similar algorithm is presented which improves the performance in the presence of amplitude variation:

$$\theta_1(n+1) = \theta_1 - e(n)x_1(n)\frac{\epsilon}{(A^2+1)(\theta_1^2\mu+1)}, \quad (13)$$

where A is the amplitude of the signal, and ϵ, μ, are positive parameters which determine the speed of adaptation, and $e(n)$ is the error signal between the input and the output of the filter.

4. ANF Normalization

In order to obtain a unity gain of the transfer functions for the orthogonal system Eq. (10) and Eq. (12), first the steady-state gain at the notch frequency must be calculated. This gain is obtained by substituting $z = e^{j\theta}$ (where θ is the utility phase of the input signal) in both transfer functions and obtaining the absolute value of the result. Then, we obtain:

$$|X_1(z)| = |X_2(z)| = \frac{|\cos\theta_1||\cos\theta_2|}{\sqrt{M^2+N^2}}, \quad (14)$$

where M and N are, respectively:

$$M = \sin\theta_1\cos\theta + \sin\theta_1\cos\theta_1\sin\theta_2 + \\ + \cos 2\theta_1 + \sin\theta_2, \quad (15)$$

$$N = \sin\theta_1\sin\theta + \sin\theta_1\sin\theta\sin\theta_2 + \sin 2\theta. \quad (16)$$

Finally, if the frequency of the input signal is the same as the notch frequency, ensuring that is $\theta = \theta_1$, which is ensured by the adaptive algorithm in Sec. 3. , then the gains reduce to:

$$|X_1(z)| = |X_2(z)| = \frac{|\cos\theta_2|}{1-\sin\theta_2}. \quad (17)$$

Dividing Eq. (10) and Eq. (12) by the gain Eq. (17), both transfer functions will have a unity gain:

$$X_1(z) = \frac{\cos\theta_1(1-\sin\theta_2)z^{-1}}{1+\sin\theta_1(1+\sin\theta_2)z^{-1}+\sin\theta_2 z^{-2}}, \quad (18)$$

$$X_2(z) = \frac{\sin\theta_1(\sin\theta_2-1)z^{-1}+(\sin\theta_2-1)z^{-2}}{1+\sin\theta_1(1+\sin\theta_2)z^{-1}+\sin\theta_2 z^{-2}}. \quad (19)$$

Figure 5, shows the structure of the APF once normalized and Fig. 6 shows the bode plot for these two transfer functions before and after normalization.

5. Implementation Issues

Although the orthonormal system generator has so far been presented as two transfer functions, the space-state representation is much more appropriate for its

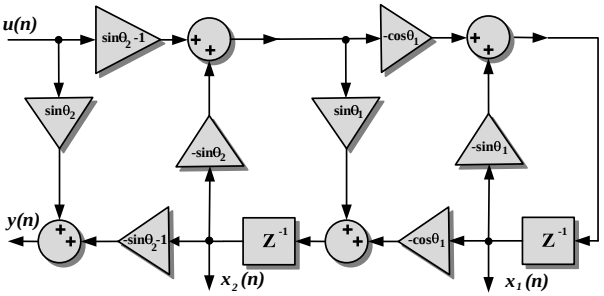
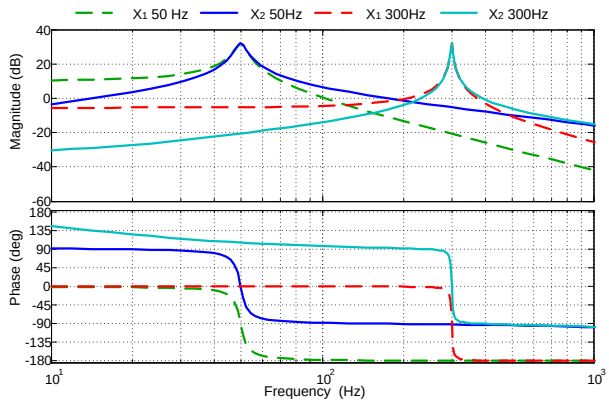
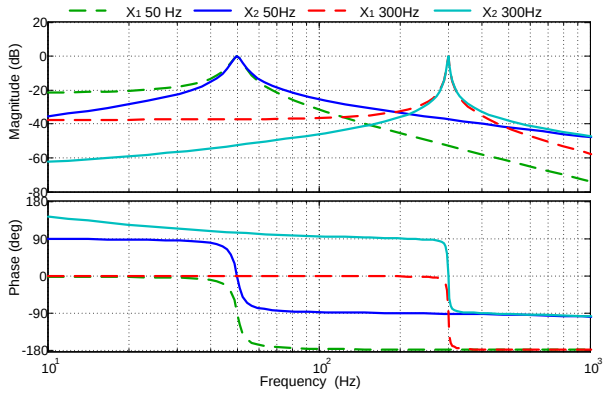


Fig. 5: APF generator of an orthogonal system with unity gain.



(a) Before normalization.



(b) After normalization.

Fig. 6: Bode plot of the transfer function of X_1 and X_2.

implementation in a DSP. The APF state-space equation before and after normalization is next given:

$$\begin{bmatrix} x_1(n+1) \\ x_2(n+1) \end{bmatrix} = \begin{bmatrix} \sin\theta_1 & \cos\theta_1 \sin\theta_2 \\ \cos\theta_1 & \sin\theta_1 \sin\theta_2 \end{bmatrix} \cdot \cdot \begin{bmatrix} x_1(n) \\ x_2(n) \end{bmatrix} + \begin{bmatrix} \cos\theta_1 \cos\theta_2 \\ \sin\theta_1 \cos\theta_2 \end{bmatrix} u(n), \tag{20}$$

$$y(n) = \begin{bmatrix} 0 & \cos\theta_2 \end{bmatrix} \begin{bmatrix} x_1(n) \\ x_2(n) \end{bmatrix} + \sin\theta_2 u(n). \tag{21}$$

The state-space equation can be rewritten in a more compact form as:

$$\begin{bmatrix} x_1(n+1) \\ x_2(n+1) \\ y(n) \end{bmatrix} = \begin{bmatrix} \sin\theta_1 & \cos\theta_1 \sin\theta_2 & \cos\theta_1 \cos\theta_2 \\ \cos\theta_1 & \sin\theta_1 \sin\theta_2 & \sin\theta_1 \cos\theta_2 \\ 0 & \cos\theta_2 & \sin\theta_2 \end{bmatrix} \cdot \begin{bmatrix} x_1(n) \\ x_2(n) \\ u(n) \end{bmatrix}, \tag{22}$$

and once normalized, we obtain:

$$\begin{bmatrix} x_1(n+1) \\ x_2(n+1) \\ y(n) \end{bmatrix} = = \begin{bmatrix} -\sin\theta_1 & \cos\theta_1 \sin\theta_2 & \cos\theta_1(1-\sin\theta_2) \\ -\cos\theta_1 & -\sin\theta_1 \sin\theta_2 & \sin\theta_1(\sin\theta_2 - 1) \\ 0 & -(1+\sin\theta_2) & \sin\theta_2 \end{bmatrix} \cdot \begin{bmatrix} x_1(n) \\ x_2(n) \\ u(n) \end{bmatrix}. \tag{23}$$

In order to calculate the updates of the two signals of the orthonormal system generator, it is sufficient to calculate the two first rows of Eq. (23). Finally, it is important to note that no special care must be taken to address a possible DC component of the input voltage signal although, unlike with the other traditional PLLs [30], the notch filtering of the APF-PLL prevents the effect of a biased input sinusoidal voltage on the orthogonal system generator. The following section shows the validity of these statements.

6. Simulation and Experimental Results

In order to prove the validity of the theoretical results in the previous sections, Matlab/Simulink simulation and experimental results are given. The set of perturbations used, namely those relevant to Institute of Electrical and Electronics Engineers (IEEE) Std. 929-2000 [38], IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems, was the same in both cases.

The variables in all the simulation and experimental results are: the single-phase voltage to the APF-PLL, the two orthogonal signals generated by the APF-PLL, the fundamental vs. estimated phase angle, and finally, depending on the perturbation, the input vs. output frequency or the input vs. output voltage amplitude. The tuning of the APF-PLL was kept constant throughout the simulations, with a notch frequency of 50 Hz, a pass band of 28 Hz, a sampling frequency of 20 kHz, $\epsilon = 0.0001$ and $\mu = 0.0001$. The set of perturbations includes:

- Frequency variation: the input to the PLL consisting of a sinusoid of frequency 50 Hz. At time 0.2 s, the frequency is changed with a step to 52 Hz. As a reference value, IEEE Std. 929-2000 states that the frequency variation rate should be no faster

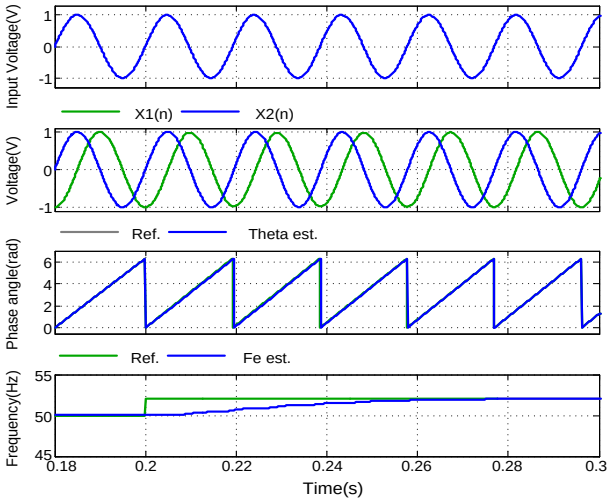
than 0.5 Hz·s^{-1}, and the delay time for the inverter to cease to energize the utility line should be no longer tan six cycles. Moreover, the frequency measurement error should be $\leq$ 0.1 Hz. Figure 7(a), shows the estimated phase angle versus reference phase angle and estimated frequency versus reference frequency. The simulation results show that, after a short transient, the APF-PLL algorithm estimates accurately the new frequency in less than 3 cycles, fulfilling the above standard.

- Voltage sag: the input to the APF-PLL consisting of a sinusoid of 50 Hz and amplitude of 1.0 p.u. At time 0.2 s, a voltage sag of 25 % is suddenly applied to the PLL. As a reference value, IEEE Std. 929-2000 states that in a voltage sag of 50 % or less, the maximum trip time of the PV inverter should be less than 6 cycles. Figure 7(b), shows the instantaneous RMS value versus reference value of the amplitude voltage. The simulation results show that, after a short transient, the APF-PLL algorithm estimates accurately the new amplitude in less than 2 cycles, fulfilling the above standard.

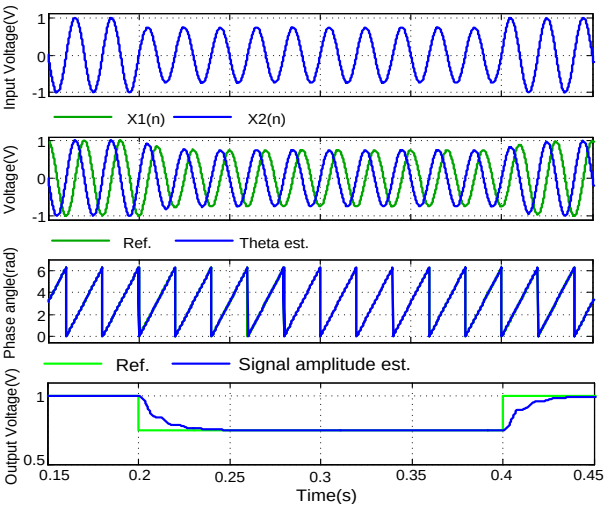
- Harmonic distortion: IEEE Std. 929-2000 states that PV inverters must withstand a certain amount of waveform distortion without specifying any value. The APF-PLL algorithm is subjected to a voltage distortion in Fig. 7(c) consisting of 25 % of the third harmonic and 15 % of the fifth harmonic. Again, no impact on the phase angle or frequency estimation is detected.

The APF-PLL presented in this paper, has been implemented in a DSP from Texas Instruments (TMS320F2812), which has a 32 bit fixed-point Central Processing Unit (CPU) with 150 Mips. This CPU is provided with a hardware multiplier, and so it can realize a multiplication and posterior addition in one single clock cycle; this is an important feature for the execution of state-space equations such as that in Eq. (23). Apart from that, a look-up table for sine and cosine calculations is located in the boot Read Only Memory (ROM) of the device, making the trigonometric calculations to be performed efficiently (the sine and cosine function for an angle, with an accuracy of 30 bits, can be executed in 60 clock cycles). The set-up consisted in a board with the aforementioned DSP, along with a 12 bit 4-channels Digital to Analog Converter (DAC) interfaced with the DSP through the SPI bus; and connected to this DAC, a Picoscope oscilloscope which plots are depicted in Fig. 8.

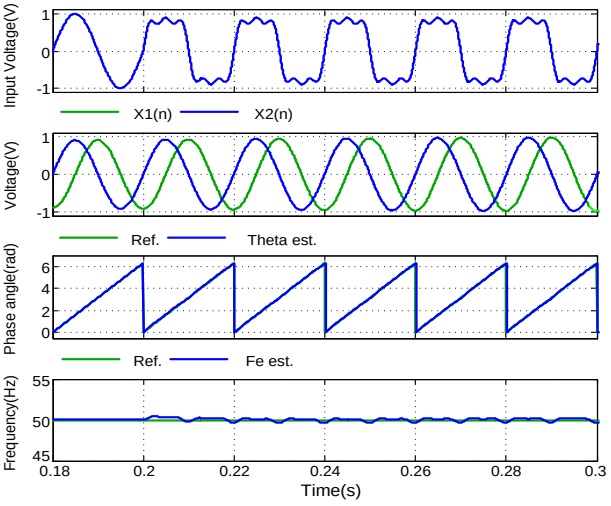
The inputs to the APF-PLL algorithm were the same as in simulation. These inputs were internally generated, through mathematical equations, so that no Analog to Digital Converter (ADC) was necessary, and in



(a) Step change in the input frequency.

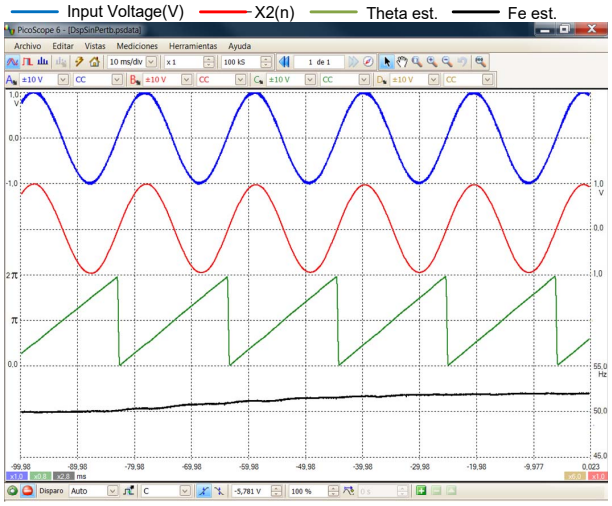


(b) Voltage sag of 25 %.

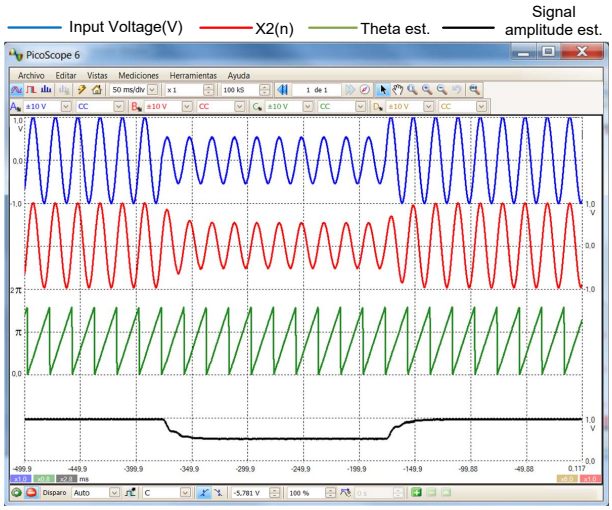


(c) Waveform distortion with 25 % of the third harmonic and 15 % of the fifth harmonic.

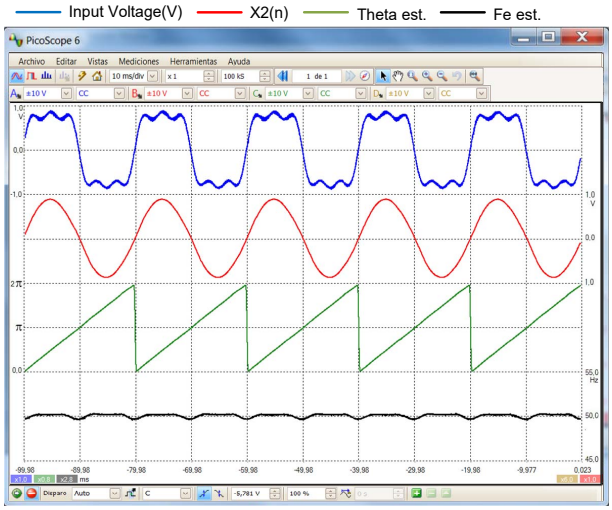
Fig. 7: Matlab/Simulink simulation results of the APF-PLL.



(a) Step change in the input frequency.



(b) Voltage sag of 25 %.



(c) Waveform distortion with 25 % of the third harmonic and 15 % of the fifth harmonic.

Fig. 8: Experimental results of the APF-PLL.

this way, avoiding any non-desired noise which could mask the output results.

In Fig. 8, there is complete consistency between the simulation outputs and those resulting from the implementation in a DSP. The APF-PLL, in all three cases implemented in the DSP, accurately estimates the $x_2(n)$ output as an input signal image, without disturbances and determines the phase angle with great precision. In Fig. 8(a), it is shown that the implementation of the APF-PLL, estimates the new frequency of 52 Hz, in less than 3 cycles, just as was done in the simulation of Fig. 7(a). In Fig. 8(b), the APF-PLL estimates, as in the simulation, the new amplitude in less than 2 cycles of the input signal. And in Fig. 8(c), the frequency achieved is identical to that of the simulation exhibited in Fig. 7(c), presenting the same variations, which are not very pronounced, being less than 0.2 Hz.

The experimental results, carried out in a DSP, have confirmed the simulation results, showing a fully satisfactory behavior of the proposed PLL in both transient and steady-state. In particular, the APF-PLL presents a considerable robustness against input signals variations and distortions; moreover, the steady-state errors on phase angle and on frequency are reduced to negligible values.

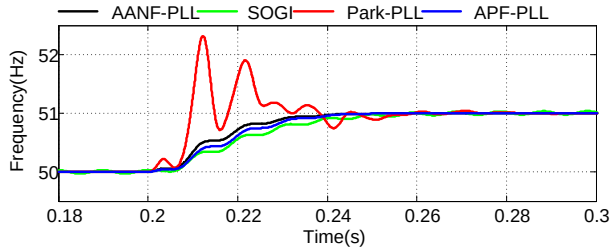
7. Comparative Study

We carried out a comparative study, by simulation, with other PLLs, the most representative ones: the Amplitude Adaptive Notch Filter (AANF) [37], SOGI [20], [24] and [27] and Park-PLL [17]. This comparison has been made regarding the estimation of the frequency and amplitude of the grid voltage under abnormal conditions.

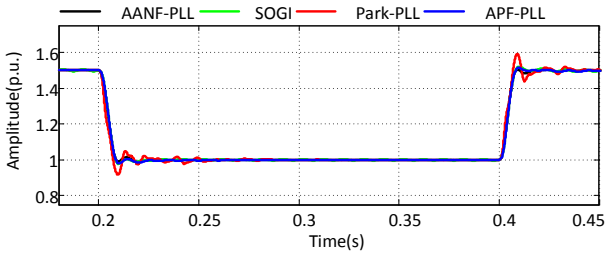
The set of perturbations used are similar to the ones of the previous section, including a frequency jump from 50 Hz to 51 Hz; a voltage sag from 1.5 p.u. to 1.0 p.u.; a phase-jump of 40 degrees; and the addition of a 25 % of the third harmonic and 15 % of the fifth harmonic. The sampling frequency is kept constant to 20 kHz.

The dynamic response of the four PLLs under +1 Hz frequency jump scenario is displayed in Fig. 9(a). It can be obtained that the AANF-PLL and APF-PLL shows the fast dynamic response of near 2 cycles, and do not produce frequency overshoot. Further, the AANF-PLL and APF-PLL have no oscillation after the frequency jump, which offers the good performance with frequency immunity, and may be the best choice under this situation among the four PLLs. The SOGI also shows a fast, but 3 cycles dynamic response with a small oscillation.

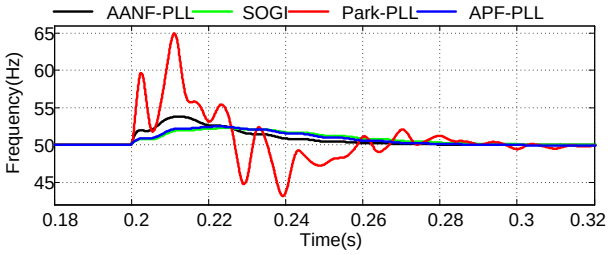
Figure 9(b) displays the simulation results scenario when the grid voltage undergoes 66.7 % voltage sag. It can be seen that the four PLLs show a similar response in estimating the voltage amplitude. With a tracking time of approximately 0.5 cycles. The APF-PLL and AANF-PLL present good behavior after the amplitude change, producing an output with minimal steady state oscillations. In contrast, the SOGI and the Park-PLL display oscillations in the estimation of the voltage amplitude.



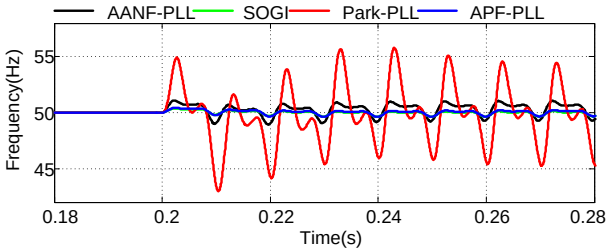
(a) Detected frequency for variation of 1 Hz.



(b) Response to an amplitude step changes.



(c) Detected frequency for phase jump of 40 degrees.



(d) Detected frequency for phase jump of 40 degrees with the presence of harmonics.

Fig. 9: Comparison of PLLs.

As is exhibited in Fig. 9(c), when the grid voltage undergoes a phase angle jump of +40 degrees, the AANF-PLL, SOGI and APF-PLL have a similar dynamic response, with a tracking time of about 3 cycles. The Park-PLL does not perform well, which takes more 5 cycles to reach the steady-state conditions and with pronounced oscillations.

Figure 9(d) offers the simulation results when the grid voltage undergoes harmonics scenario. The harmonics have almost no influence on SOGI and APF-PLL thanks to their filter properties. But the ANNF-PLL and Park-PLL show noticeable oscillations greater than 1 Hz and 4 Hz, respectively.

In Fig. 9, the comparative results are presented. One can observe that the APF-PLL, the AANF-PLL (being a closed continuous time implementation of the APF-PLL) and the SOGI exhibit similar performance in all the four simulations. It is possible to verify that the APF-PLL, in addition to providing good work with low frequency pass, amplitude change, phase pass and good harmonic rejection, has the notable advantage of its simplicity.

8. Conclusion

A new orthogonal system based on an APF with Lattice structure has been proposed. This structure was presented and its discrete algorithm has been detailed. The Lattice APF generates an identical signal and another signal orthogonal to the input fundamental signal, without disturbances since the orthogonal system is filtered without delay by the same structure due to resonance at the fundamental frequency. This proposed orthogonal system, according to its characteristics and behavior, is ideal to be used as a single-phase PLL.

A single PLL based on an ANF is presented and behavior and implementation issues are analyzed in detail. The APF-PLL, has shown the ability to generate an orthogonal system from a single phase signal, with unity gain, which does not depend on the 3 dB pass-band of the filter and does not depend on the frequency as it is adaptive to it, maintaining high linearity and great filtering power. Despite its simple design, it uses few resources to implement in a fixed-point DSP, it requires only 6 multiplications plus accumulations, the APF-PLL provides great precision and low sensitivity to coefficient rounding (due to its internal structure) while exhibiting good response to frequency variations, voltage sags and harmonic distortion. The APF-PLL does not present considerable amplitude ripples and phase delays for the generated quadrature signal. These results have been confirmed by simulations and an experimental setup.

References

[1] TAUL, M. G., X. WANG, P. DAVARI and F. BLAABJERG. An Overview of Assessment Methods for Synchronization Stability of Grid-Connected Converters Under Severe Symmetrical Grid Faults. *IEEE Transactions on Power Electronics*. 2019, vol. 34, iss. 10, pp. 9655–9670. ISSN 1941-0107. DOI: 10.1109/TPEL.2019.2892142.

[2] AHMED, H., M. BENBOUZID, M. AHSAN, A. ALBARBAR and M. SHAHJALAL. Frequency Adaptive Parameter Estimation of Unbalanced and Distorted Power Grid. *IEEE Access*. 2020, vol. 8, iss. 1, pp. 8512–8519. ISSN 2169-3536. DOI: 10.1109/ACCESS.2020.2964058.

[3] ABOUDRAR, I., S. EL HANI, H. MEDIOUNI and A. AGHMADI. Modeling and Robust Control of a Grid Connected Direct Driven PMSG Wind Turbine By ADRC. *Advances in Electrical and Electronic Engineering*. 2018, vol. 16, iss. 4, pp. 402–413. ISSN 1804-3119. DOI: 10.15598/aeee.v16i4.2952.

[4] CAMACHO, A., M. CASTILLA, J. MIRET, L. G. DE VICUNA and G. L. M. ANDRES. Control Strategy for Distribution Generation Inverters to Maximize the Voltage Support in the Lowest Phase During Voltage Sags. *IEEE Transactions on Industrial Electronics*. 2018, vol. 65, iss. 3, pp. 2346–2355. ISSN 1557-9948. DOI: 10.1109/TIE.2017.2736486.

[5] HU, X. and K.-J. TSENG. Integration of Multiple Modularized Distributed Energy Resource Devices Into AC Grid of Buildings: Issue of Active Power Circulation. *IEEE Transactions on Industrial Electronics*. 2014, vol. 61, iss. 11, pp. 6118–6127. ISSN 1557-9948. DOI: 10.1109/TIE.2014.2304924.

[6] ECHCHAACHOUAI, A., S. EL HANI, A. HAMMOUCH and I. ABOUDRAR. A Two-Level Sensorless MPPT Strategy Using SRF-PLL on a PMSG Wind Energy Conversion System. *Advances in Electrical and Electronic Engineering*. 2017, vol. 15, iss. 3, pp. 383–390. ISSN 1804-3119. DOI: 10.15598/aeee.v15i3.2215.

[7] CHANG, C.-H., Y.-H. LIN, Y.-M. CHEN and Y.-R. CHANG. Simplified Reactive Power Control for Single-Phase Grid-Connected Photovoltaic Inverters. *IEEE Transactions on Industrial Electronics*. 2014, vol. 61, iss. 5, pp. 2286–2296. ISSN 1557-9948. DOI: 10.1109/TIE.2013.2271600.

[8] BLAABJERG, F., R. TEODORESCU, M. LISERRE and A. V. TIMBUS. Overview of Control and Grid Synchronization for Distributed Power Generation Systems. *IEEE Transactions on Industrial Electronics*. 2006, vol. 53, iss. 10, pp. 1398–1409. ISSN 1557-9948. DOI: 10.1109/TIE.2006.881997.

[9] GOLESTAN, S., J. M. GUERRERO and J. C. VASQUEZ. Three-Phase PLLs: A Review of Recent Advances. *IEEE Transactions on Power Electronics*. 2017, vol. 32, iss. 3, pp. 1894–1907. ISSN 1941-0107. DOI: 10.1109/TPEL.2016.2565642.

[10] ESTEBANEZ, E. J., V. M. MORENO, A. PIGAZO, M. LISERRE and A. DELLAQUILA. Performance Evaluation of Active Islanding-Detection Algorithms in Distributed-Generation Photovoltaic Systems: Two Inverters Case. *IEEE Transactions on Industrial Electronics*. 2011, vol. 58, iss. 4, pp. 1185–1193. ISSN 1557-9948. DOI: 10.1109/TIE.2010.2044132.

[11] VASQUEZ, J. C., J. M. GUERRERO, M. SAVAGHEBI, J. ELOY-GARCIA and R. TEODORESCU. Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters. *IEEE Transactions on Industrial Electronics*. 2013, vol. 60, iss. 4, pp. 1271–1280. ISSN 1557-9948. DOI: 10.1109/TIE.2012.2194951.

[12] HAN, Y., M. LUO, X. ZHAO, J. M. GUERRERO and L. XU. Comparative Performance Evaluation of Orthogonal-Signal-Generators-Based Single-Phase PLL Algorithms—A Survey. *IEEE Transactions on Power Electronics*. 2016, vol. 31, iss. 5, pp. 3932–3944. ISSN 1941-0107. DOI: 10.1109/TPEL.2015.2466631.

[13] MONFARED, M., S. GOLESTAN and J. M. GUERRERO. Analysis, Design, and Experimental Verification of a Synchronous Reference Frame Voltage Control for Single-Phase Inverters. *IEEE Transactions on Industrial Electronics*. 2014, vol. 61, iss. 1, pp. 258–269. ISSN 1557-9948. DOI: 10.1109/TIE.2013.2238878.

[14] ELRAYYAH, A., Y. SOZER and M. ELBULUK. Robust phase locked-loop algorithm for single-phase utility-interactive inverters. *IET Power Electronics*. 2014, vol. 7, iss. 5, pp. 1064–1072. ISSN 1755-4535. DOI: 10.1049/iet-pel.2013.0351.

[15] TAN, G., X. SUN, X. LI, A. WANG and P. WANG. Orthogonal Decoupling Control of the Error of a New-Type Phase-Locked Loop under Unbalanced Grid Conditions. In: *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*. Shenzhen:

IEEE, 2018, pp. 1–7. ISBN 978-1-5386-6054-6. DOI: 10.1109/PEAC.2018.8590241.

[16] GOLESTAN, S., M. RAMEZANI, J. M. GUERRERO, F. D. FREIJEDO and M. MONFARED. Moving Average Filter Based Phase-Locked Loops: Performance Analysis and Design Guidelines. *IEEE Transactions on Power Electronics*. 2014, vol. 29, iss. 6, pp. 2750–2763. ISSN 1941-0107. DOI: 10.1109/TPEL.2013.2273461.

[17] NAYAK, S., S. GURUNATH and N. RAJASEKAR. Advanced single-phase inverse park PLL with tuning of PI controller for improving stability of grid utility using soft computing technique. In: *2016 Online International Conference on Green Engineering and Technologies (IC-GET)*. Coimbatore: IEEE, 2016, pp. 1–5. ISBN 978-1-5090-4556-3. DOI: 10.1109/GET.2016.7916732.

[18] ELRAYYAH, A., A. SAFAYET, Y. SOZER, I. HUSAIN and M. ELBULUK. Efficient Harmonic and Phase Estimator for Single-Phase Grid-Connected Renewable Energy Systems. *IEEE Transactions on Industry Applications*. 2014, vol. 50, iss. 1, pp. 620–630. ISSN 1939-9367. DOI: 10.1109/TIA.2013.2266392.

[19] GOLESTAN, S., M. MONFARED, F. D. FREIJEDO and J. M. GUERRERO. Dynamics Assessment of Advanced Single-Phase PLL Structures. *IEEE Transactions on Industrial Electronics*. 2013, vol. 60, iss. 6, pp. 2167–2177. ISSN 1557-9948. DOI: 10.1109/TIE.2012.2193863.

[20] CIOBOTARU, M., R. TEODORESCU and F. BLAABJERG. A new single-phase PLL structure based on second order generalized integrator. In: *2006 37th IEEE Power Electronics Specialists Conference*. Jeju: IEEE, 2006, pp. 1–6. ISBN 0-7803-9716-9. DOI: 10.1109/PESC.2006.1711988.

[21] RODRIGUEZ, P., A. LUNA, M. CIOBOTARU, R. TEODORESCU and F. BLAABJERG. Advanced Grid Synchronization System for Power Converters under Unbalanced and Distorted Operating Conditions. *In: IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*. Paris: IEEE. 2006, pp. 5173–5178. ISBN 978-1-5090-9155-3. DOI: 10.1109/IECON.2006.347807.

[22] RODRIGUEZ, P., A. LUNA, I. CANDELA, R. MUJAL, R. TEODORESCU and F. BLAABJERG. Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions. *IEEE Transactions on Industrial Electronics*. 2011, vol. 58, iss. 1, pp. 127–138. ISSN 1557-9948. DOI: 10.1109/TIE.2010.2042420.

[23] MERAL, M. E. and D. CELIK. DSOGI-PLL Based Power Control Method to Mitigate Control Errors Under Disturbances of Grid Connected Hybrid Renewable Power Systems. *Advances in Electrical and Electronic Engineering*. 2018, vol. 16, iss. 1, pp. 81–91. ISSN 1804-3119. DOI: 10.15598/aeee.v16i1.2485.

[24] TAGHIZADEH, S., M. J. HOSSAIN and J. LU. Enhanced orthogonal signal generator for a single-phase grid-connected converter. *IET Power Electronics*. 2018, vol. 11, iss. 15, pp. 2563–2572. ISSN 1755-4535. DOI: 10.1049/iet-pel.2018.5253.

[25] JORGE, S. G., J. A. SOLSONA and C. A. BUSADA. Control Scheme for a Single-Phase Grid-Tied Voltage Source Converter With Reduced Number of Sensors. *IEEE Transactions on Power Electronics*. 2014, vol. 29, iss. 7, pp. 3758–3765. ISSN 1941-0107. DOI: 10.1109/TPEL.2013.2278493.

[26] MATAS, J., H. MARTIN, J. DE LA HOZ, A. ABUSORRAH, Y. AL-TURKI and H. AL-SHAEIKH. A New THD Measurement Method With Small Computational Burden Using a SOGI-FLL Grid Monitoring System. *IEEE Transactions on Power Electronics*. 2020, vol. 35, iss. 6, pp. 5797–5811. ISSN 1941-0107. DOI: 10.1109/TPEL.2019.2953926.

[27] SI, Y., Y. LIU, C. LIU, Z. ZHANG and Q. LEI. Reactive Power Injection and SOGI Based Active Anti-Islanding Protection Method. In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. Baltimore: IEEE, 2019, pp. 2637–2642. ISBN 978-1-7281-0395-2. DOI: 10.1109/ECCE.2019.8912539.

[28] RIVAS, H. A. and J. BERGAS. Frequency Determination in a Single-Phase Voltage Signal using Adaptative Notch Filters. In: *2007 9th International Conference on Electrical Power Quality and Utilisation*. Barcelona: IEEE, 2007, pp. 1–7. ISBN 978-8-4690-9441-9. DOI: 10.1109/EPQU.2007.4424151.

[29] GOLESTAN, S., J. M. GUERRERO, F. MUSAVI and J. C. VASQUEZ. Single-Phase Frequency-Locked Loops: A Comprehensive Review. *IEEE Transactions on Power Electronics*. 2019, vol. 34, iss. 12, pp. 11791–11812. ISSN 1941-0107. DOI: 10.1109/TPEL.2019.2910247.

[30] KARIMI-GHARTEMANI, M., S. A. KHAJEHODDIN, P. K. JAIN, A. BAKHSHAI and M. MOJIRI. Addressing DC Component in PLL and Notch Filter Algorithms. *IEEE Transactions on Power Electronics*. 2012,

vol. 27, iss. 1, pp. 78–86. ISSN 1941-0107. DOI: 10.1109/TPEL.2011.2158238.

[31] REGALIA, P. A., S. K. MITRA and P. P. VAIDYANATHAN. The digital all-pass filter: a versatile signal processing building block. *Proceedings of the IEEE*. 1988, vol. 76, iss. 1, pp. 19–37. ISSN 1558-2256. DOI: 10.1109/5.3286.

[32] SUBRAMANIAN, C. and R. KANAGARAJ. Single-Phase Grid Voltage Attributes Tracking for the Control of Grid Power Converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2014, vol. 2, iss. 4, pp. 1041–1048. ISSN 2168-6785. DOI: 10.1109/JESTPE.2014.2341045.

[33] REGALIA, P. A. An improved lattice-based adaptive IIR notch filter. *IEEE Transactions on Signal Processing*. 1991, vol. 39, iss. 9, pp. 2124–2128. ISSN 1941-0476. DOI: 10.1109/78.134453.

[34] GONZALEZ-ESPIN, F., E. FIGUERES and G. GARCERA. An Adaptive Synchronous-Reference-Frame Phase-Locked Loop for Power Quality Improvement in a Polluted Utility Grid. *IEEE Transactions on Industrial Electronics*. 2012, vol. 59, iss. 6, pp. 2718–2731. ISSN 1557-9948. DOI: 10.1109/TIE.2011.2166236.

[35] COUSSEAU, J. E., S. WERNER and P. D. DONATE. Factorized All-Pass Based IIR Adaptive Notch Filters. *IEEE Transactions on Signal Processing*. 2007, vol. 55, iss. 11, pp. 5225–5236. ISSN 1941-0476. DOI: 10.1109/TSP.2007.898778.

[36] REGALIA, P. A. Stable and efficient lattice algorithms for adaptive IIR filtering. *IEEE Transactions on Signal Processing*. 1992, vol. 40, iss. 2, pp. 375–388. ISSN 1941-0476. DOI: 10.1109/78.124947.

[37] YIN, G., L. GUO and X. LI. An Amplitude Adaptive Notch Filter for Grid Signal Processing. *IEEE Transactions on Power Electronics*. 2013, vol. 28, iss. 6, pp. 2638–2641. ISSN 1941-0107. DOI: 10.1109/TPEL.2012.2226752.

[38] IEEE Std. 929-2000. *IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*. New York: IEEE, 2000.

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Appendix A Nomenclature

PCC	Point of Common Coupling
PV	Solar Photovoltaic
IIR	Infinite Impulse Response
$A(z)$	All-pass filter transfer function
$F(z)$	Notch filter transfer function
$G(z)$	Band-pass filter transfer function
$X_1(z)$	Quadrature signal transfer function
$X_2(z)$	Phase signal transfer function
ω	Angular frequency
θ	Utility phase of the input signal
ω_0	Notch frequency
BW	Band width of the filter
B	Band pass
f_s	Sampling frequency
f_e	Estimated frequency
$u(n)$	Input signal
$y_f(n)$	Output filtered
$x_1(n)$, $x_2(n)$	Orthogonal components